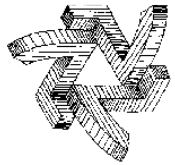

MINOS Near Detector
Front End Electronics Tutorial

Description of the MINDER Module

Presented By

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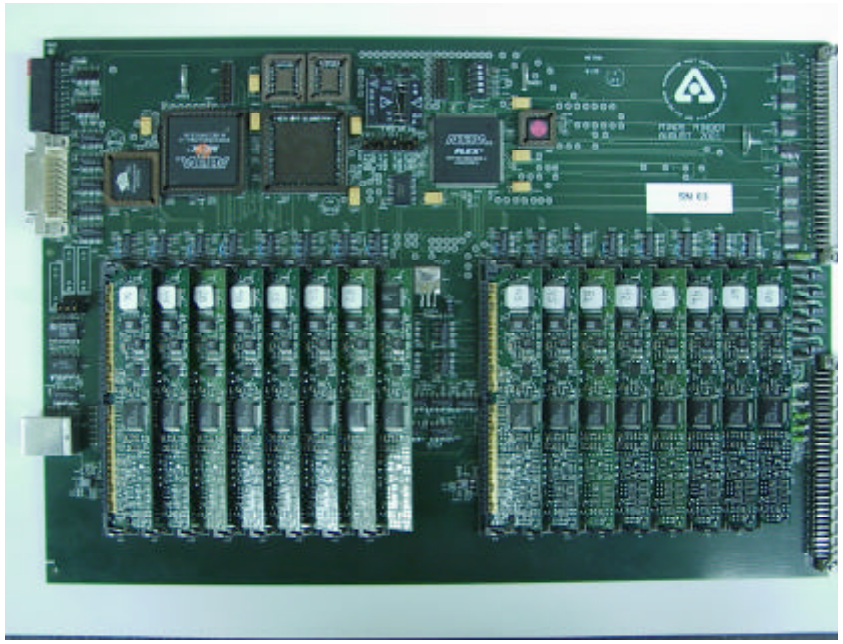
Description of MINDER

Overview

- **Some Background**

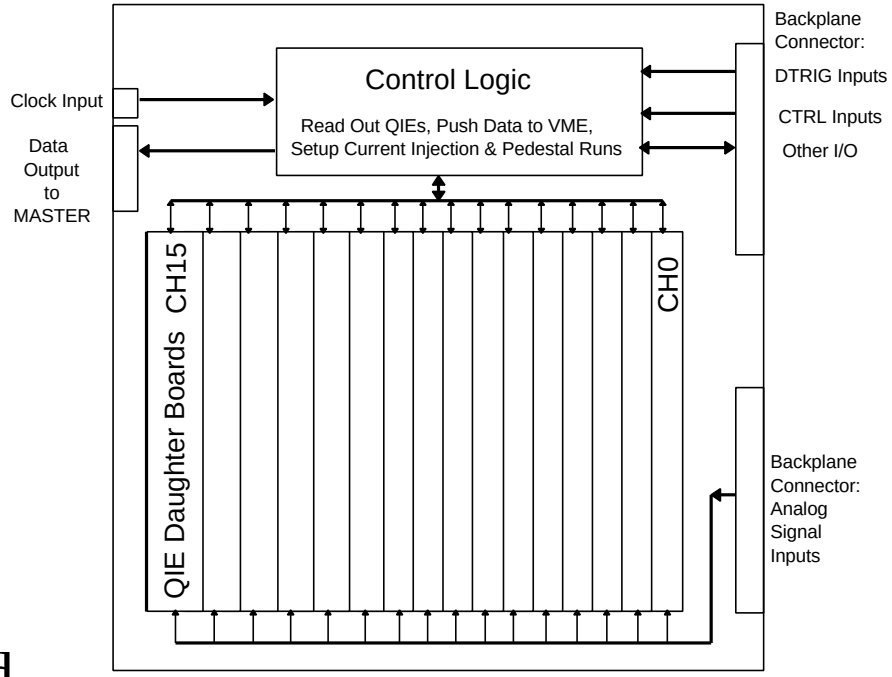
  - Similar to CDF Shower Max Design (SMD)
  - 6U Format
  - Holds 16 MENU Modules
  - (1/4) 16-Channel PMT
  - Reside in Crates Close to Photodetectors



Description of MINDER

Overview (Cont.)

- **What it Does (Cont.)**
  - Processes Triggers
  - Pushes Data to MASTER
  - Contains 27-Bit Timestamp Counters
  - Sets Up DC Current Calibration
  - Contains Pre-Programmed Diagnostic Data



Description of MINDER

Timing

- Every MINDER has Point-to-Point Connection with MTM to Receive Timing Signals:
  - QCLK - 53 MHz for QIE
  - SGATE - Spill Gate for Spill in Progress
  - CNTRST - Timestamp Counter Reset
  - TCAL - Used for Diagnostics

Description of MINDER

Triggering

- **General Philosophy**
  - SGATE Comes from MTM
  - Other Trigger Signals Come in from KEEPER Across Backplane as nDTRIG, on Dedicated Signal Lines
    - Dynode Trigger (Cosmic Rays, Dark Current)
    - VME Trigger
    - Flash Trigger
    - External Process

Description of MINDER

Triggering (Cont.)

- **Spill Gate Trigger**
  - SGATE Comes from Clock System via MTM
  - Causes Writing of Data to FIFOs on MENU Module for Duration of Gate (10 uSec ~ 526 Clocks)
  - Data Read Out After Spill
  - Data Marked as Spill Data

Description of MINDER

Triggering (Cont.)

- **Dynode Trigger**
  - Comes from Discriminators on KEEPER
  - Discriminated Signal from All 4 PMTs Sent from KEEPER Onto Backplane as nDTRIG[3:0]
  - MINDERS Receive All 4 Signals
  - Slot Switch Settings on MINDER Tell It Which nDTRIG Signal to Respond To

    →***MUST*** Set Address Switches Properly

Description of MINDER

Triggering (Cont.)

- **Dynode Trigger (Cont.)**
  - Causes Writing of Data to FIFOs on MENU Module for 8 Clocks
  - Data Read Out After Write Cycle
  - Data Marked as Dynode Event

Description of MINDER

Triggering (Cont.)

- **Dynode Trigger (Cont.)**
  - Setting Switches on MINDER:
    - Address Switched on MINDER Correspond to Slot
    - Switches Control Which of Dynode Signals (nDTRIG0 - nDTRIG3) to Respond To

Slot	nDTRIG
0- 2	None
3- 6	nDTRIG0
7-10	nDTRIG1
11-14	nDTRIG2
15-18	nDTRIG3
19-21	None

Description of MINDER

Triggering (Cont.)

- **VME Trigger**
  - Issued by ROP through MASTER to KEEPER
  - Used to Obtain Pedestal and Calibration (ICAL) Events
  - KEEPER Sends Onto Backplane as nDTRIG6
  - MINDERS Programmed to Acquire 64 Clock Cycles
  - Causes Writing of Data to FIFOs on MENU Module for 64 Clocks
  - Data Read Out After Write Cycle
  - Data Marked as Pedestal Event or ICAL Event

Description of MINDER

Triggering (Cont.)

- **Flash Event Trigger**
  - Comes from TCAL on KEEPER
  - KEEPER Sends Onto Backplane as nDTRIG4
  - KEEPER Looks for Coincidence of This ***and*** Dynode Trigger
  - Causes Writing of Data to FIFOs on MENU Module for 8 Clocks
  - Data Read Out After Write Cycle
  - No Different from Normal Dynode Trigger ***Except*** Event is Marked as Flash Event

Description of MINDER

Triggering (Cont.)

- **External Process Trigger**
  - Comes from Front Panel Connector on KEEPER
  - KEEPER Sends Onto Backplane as nDTRIG5
  - Causes Writing of Data to FIFOs on MENU Module for 8 Clocks
  - Data Read Out After Write Cycle
  - Data Marked as External Process Event

Description of MINDER

Triggering (Cont.)

- **Summary of Triggering**

Trigger	Meaning	Used For
SGATE	Spill Gate	Trigger on Spill
nDTRIG[3:0]	Dynode Trigger	Cosmic Rays, PMT Noise, Flasher
nDTRIG4	Flasher Trigger	Forms Gate with Dynode Trigger
nDTRIG5	External Process	Tests, Special Applications
nDTRIG6	VME Trigger	Pedestals, Calibrations

Description of MINDER

Controlling the Triggering

- **General Philosophy**
  - There Exists 8 Dedicated Control Lines on Backplane, Set by MASTER Writing Register to KEEPER
  - Called nCTRL[7:0]
  - First 3, nCTRL[2:0] Set Mode - 8 States
    - 1 State for Physics
    - 6 States for “Utilities”
    - 1 Off State
  - Remaining 5 States Used for Physics

Description of MINDER

Controlling the Triggering (Cont.)

- **CTRL Bits Defined**

CTRL[7:0]: - Set by Writing to Register on KEEPER

7 6 5 4 3 210
XXXXXnnn - nnn Are Mode Bits

When Set to - Then Module Responds
XXXXX001 to Other CTRL Bits,
Otherwise X's Ignored

Mode		Meaning	Used For
000	0	OFF	Board Will Not Respond toTriggers
001	1	NORM Mode	Physics Uses nCTRL3-nCTRL7
010	2	PED Mode	Acquire Pedestals Uses VME Trigger
011	3	ICAL Mode	DC I Inj. Cal Uses VME Trigger
100	4	DIAG Mode	Diagnostic Event Uses VME Trigger
101	5	TCAL Trig 1	Trigger on TCAL DTRIG Sequence
110	6	TCAL Trig 2	Trigger on TCAL SGATE Sequence
111	7	QIE Reset	Generate QIE Reset Using TCAL

Description of MINDER

Controlling the Triggering (Cont.)

- **CTRL Bits Defined (Cont.)**

Meaning of Other CTRL Bits:

CTRL[7:0]: - Set by Writing to Register on KEEPER

7 6 5 4 3 210
XXXXXnnn - nnn Are Mode Bits

When Set to:
XXXXX001 - Defines NORM Mode (Physics)
Then Module Respond to Other CTRL Bits,
Otherwise X's Ignored

nCTRL	Meaning	Used For
nCTRL0	Mode Bit 0	Setting Mode
nCTRL1	Mode Bit 1	Setting Mode
nCTRL2	Mode Bit 2	Setting Mode
nCTRL3	SGATE Enable	Allow Response to SGATE - Norm Mo
nCTRL4	Dynode Trigger Enable	Allow Response to Dynode - Norm Mo
nCTRL5	Ext. Flash Trigger Enable	Allow Response to Ext Flash - Norm M
NCTRL6	TCAL Flash Enable	Allow Response to TCAL Flash Trig - Norm Mode
nCTRL7	Ext. Process Enable	Allow Response to Ext. Process Trig - Norm Mode

Description of MINDER

Controlling the Triggering (Cont.)

- **CTRL Bits Defined (Cont.)**

When Set to:
XXXXX001 - Defines NORM Mode (Physics)
Then Module Respond to Other CTRL Bits, Otherwise X's Ignored

Notice that Can Individually Turn On and Off Any of Triggers in NORM Mode

nCTRL	Meaning	Used For
nCTRL0	Mode Bit 0	Setting Mode
nCTRL1	Mode Bit 1	Setting Mode
nCTRL2	Mode Bit 2	Setting Mode
nCTRL3	SGATE Enable	Allow Response to SGATE - Norm Mo
nCTRL4	Dynode Trigger Enable	Allow Response to Dynode - Norm Mo
nCTRL5	Ext. Flash Trigger Enable	Allow Response to Ext Flash - Norm M
NCTRL6	TCAL Flash Enable	Allow Response to TCAL Flash Trig - Norm Mode
nCTRL7	Ext. Process Enable	Allow Response to Ext. Process Trig - Norm Mode

Description of MINDER

Marking Data Words

- **General Philosophy**
  - Spill Events Marked by SGATE
  - Dynode Trigger Events Marked by nDTRIG[3:0]
  - Flash Events Marked by nDTRIG4
  - External Process Events Marked by nDTRIG5
  - Pedestal Events Marked by nDTRIG6 ***and No*** ICAL Enable (No Mode 3)
  - Calibration Events Marked by nDTRIG6 ***and*** ICAL Enabled (Mode 3 Set)

Description of MINDER

Marking Data Words

- **How is Data Marked?**
  - Each Data Transmission Sequence from MINDER has a Header Word
  - 3 Bits in Header Word Indicate Data Type

Description of MINDER

Marking Data Words (Cont.)

- **How is Data Marked?**

  - Data Type in Header Word Determined by What is Enabled (The nCTRL Bits), and What Kind of Trigger Was Received (The nDTRIG Bits)

Data Type	Meaning	Set By
0	Pedestal	MODE[2:0] = 2 and nDTRIG6
1	ICAL	MODE [2:0] = 3 and nDTRIG6
2	Diagnostic	MODE [2:0] = 4 and nDTRIG6
3	TCAL (Not Flasher)	MODE [2:0] = 5 and nDTRIG6
4	Spill	MODE [2:0] = 1 and SGATE
5	Dynode	MODE [2:0] = 1 and nDTRIG*i*
6	Flasher	MODE [2:0] = 1 and nDTRIG*i*
7	Ext. Process	MODE [2:0] = 1 and nDTRIG5

Description of MINDER

Diagnostic Data

- **General Philosophy**

➢MINDER Has Read-Only Memory, Pre-Programmed with Diagnostic Data

CTRL[7:0]: - Set by Writing to Register on KEEPER

7 6 5 4 3 210
XXXXXnnn - nnn Are Mode Bits

When Set to - Then Module Sends
XXXXX100 Diagnostic Data to MASTER when Triggerd from VME

Mode		Meaning	Used For
000	0	OFF	Board Will Not Respond toTriggers
001	1	NORM Mode	Physics Uses nCTRL3-nCTRL7
010	2	PED Mode	Acquire Pedestals Uses VME Trigger
011	3	ICAL Mode	DC I Inj. Cal Uses VME Trigger
100	**4**	**DIAG Mode**	**Diagnostic Event Uses VME Trigger**
101	5	TCAL Trig 1	Trigger on TCAL DTRIG Sequence
110	6	TCAL Trig 2	Trigger on TCAL SGATE Sequence
111	7	QIE Reset	Generate QIE Reset Using TCAL

Description of MINDER

Timestamps

- **General Philosophy**

  - Each MINDER Contains a 27-Bit Counter
  - Counter is Reset by CNTRST from Clock
    - All MINDERs Reset Simultaneously
  - Counter Advances with QCLK at 53 MHz
  - When Get A Trigger, Value of Counter is Stored in a Register
    - → Forms Timestamp Fiducial for Event
  - Timestamp is Sent with Data as Part of Header Words in Data Transmission
  - MASTER Uses Fiducial to Form Individual Timestamps

Description of MINDER

Data Transmission

- **General Philosophy**

  - After Trigger, Sequencer Runs that Controls Data Transmission
  - Data Sent As:

    13 Data Bits
    1 Parity Bit
    1 Header Bit
    1 Trailer Bit
    1 Error Bit
    1 Data Strobe

  - First 3 Words Are Header Bits
    - Data Bits Contain Timestamp & Data Type
    - First Word has Header Bit Set
  - Following Words Contain QIE Channel Data
    - Last Word Has Trailer Bit Set
  - MINDER Forms Parity Bit on Data Sent
  - MINDER Sends Data Strobe with Data

Description of MINDER

Data Transmission (Cont.)

- **Format**
  - ➢13 Bit Header Words:

Word	Bits: 12 11 10 09 08 07 06	05 04 03	02 01	00
1	Undefined (Set Low)	Data Type	Undefined (Set Low)	Timestamp MSB
2	Timestamp High Word (13 Bits)			
3	Timestamp Low Word (13 Bits)			

  - ➢13 Bit Data Words:

12 11	10 09 08	07 06 05 04 03 02 01 00
CAPID Bits	Range Bits	QIE ADC Bits

Description of MINDER

Data Transmission (Cont.)

- **Transmission Sequence**
  - Channel Data is Sent to MASTER Ordered in Time:

CH00, TS00
CH01, TS00
CH02, TS00
...
CH15, TS00

CH00, TS01
CH01, TS01
CH02, TS01
...

CH15, TSnn

where nn is : ~8 for cosmic ray data
~526 for STE spill data
~64 for VME Triggers

Description of MINDER

Priority Triggering

- **The Problem**
  - Data Transmission from DTRIG Takes ~4.8 uSec = 256 RF Clock
  - Spill or Flash Can Come At Any Time
  - Need Method to Interrupt Lesser Important Processes
  - 3 Levels of Priority, Used in NORM Mode Only
  - Higher Priority Process Can Interrupt Lesser One

Description of MINDER

Priority Triggering (Cont.)

- **The Solution**

Priority	Meaning	Can Interrupt:
3	- Lowest Priority - Used for Dynode	- None - Ignored if Another Priority 1 in Progress
2	- 2nd Priority - Used Flasher & Ext. Proc.	- Priority 3 - Ignored if Another Priority 2 in Progress
1	- Highest Priority - Used for Spill	- Priority 2 & Priority 3 - Ignored if Another Priority 1 in Progress
N/A	- Pedestals, ICAL Diagnostic Mode, TCAL-Generated Event	- Does Not Interrupt - Cannot Be Interrupted - Ignores Triggers if in Progress

Description of MINDER

Priority Triggering (Cont.)

- **The Solution (Cont.)**
  - When Transmission is Interrupted, MINDER Sets Priority Error Bit
    - Tells MASTER Have Premature Termination
    - Prevents Word Count Error in MASTER
  - Data Sent As:

    13 Data Bits
    1 Parity Bit
    1 Header Bit
    1 Trailer Bit
    1 Error Bit
    1 Data Strobe